

FEATURES

- Low Noise, 80 nV p-p (0.1 Hz to 10 Hz)**
 $3 \text{ nV}/\sqrt{\text{Hz}} @ 1 \text{ kHz}$
- Low Drift, 0.2 $\mu\text{V}/^\circ\text{C}$**
- High Speed, 17 V/ μs Slew Rate**
63 MHz Gain Bandwidth
- Low Input Offset Voltage, 10 μV**
- Excellent CMRR, 126 dB (Common-Voltage @ 11 V)**
- High Open-Loop Gain, 1.8 Million**
- Replaces 725, OP-07, SE5534 In Gains > 5**
- Available in Die Form**

GENERAL DESCRIPTION

The OP37 provides the same high performance as the OP27, but the design is optimized for circuits with gains greater than five. This design change increases slew rate to 17 V/ μs and gain-bandwidth product to 63 MHz.

The OP37 provides the low offset and drift of the OP07 plus higher speed and lower noise. Offsets down to 25 μV and a maximum drift of 0.6 $\mu\text{V}/^\circ\text{C}$ make the OP37 ideal for precision instrumentation applications. Exceptionally low noise ($e_n = 3.5 \text{ nV}/\sqrt{\text{Hz}}$ @ 10 Hz), a low 1/f noise corner frequency of 2.7 Hz, and the high gain of 1.8 million, allow accurate high-gain amplification of low-level signals.

The low input bias current of 10 nA and offset current of 7 nA are achieved by using a bias-current cancellation circuit. Over the military temperature range this typically holds I_B and I_{OS} to 20 nA and 15 nA respectively.

The output stage has good load driving capability. A guaranteed swing of 10 V into 600 Ω and low output distortion make the OP37 an excellent choice for professional audio applications.

PSRR and CMRR exceed 120 dB. These characteristics, coupled with long-term drift of 0.2 $\mu\text{V}/\text{month}$, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

Low-cost, high-volume production of the OP37 is achieved by using on-chip zener-zap trimming. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

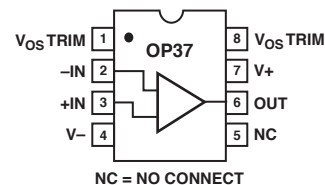
The OP37 brings low-noise instrumentation-type performance to such diverse applications as microphone, tapehead, and RIAA phono preamplifiers, high-speed signal conditioning for data acquisition systems, and wide-bandwidth instrumentation.

PIN CONNECTIONS

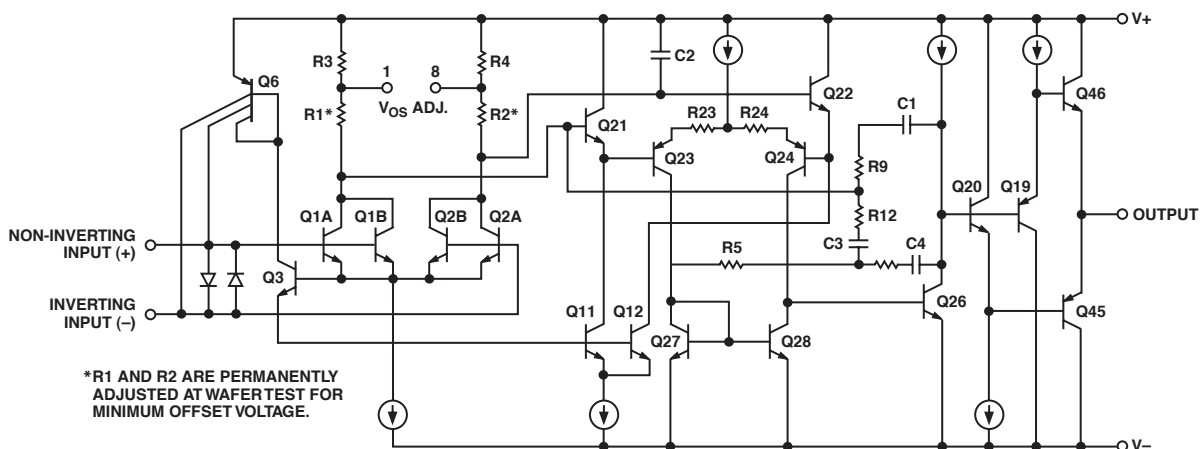
8-Lead Hermetic DIP
(Z Suffix)

Epoxy Mini-DIP
(P Suffix)

8-Lead SO
(S Suffix)



SIMPLIFIED SCHEMATIC



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OP37

ABSOLUTE MAXIMUM RATINGS⁴

Supply Voltage	22 V
Internal Voltage (Note 1)	22 V
Output Short-Circuit Duration	Indefinite
Differential Input Voltage (Note 2)	0.7 V
Differential Input Current (Note 2)	25 mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
OP37A	-55°C to +125°C
OP37E (Z)	-25°C to +85°C
OP37E, OP-37F (P)	0°C to 70°C
OP37G (P, S, Z)	-40°C to +85°C
Lead Temperature Range (Soldering, 60 sec)	300°C
Junction Temperature	-45°C to +150°C

Package Type	θ_{JA}^3	θ_{JC}	Unit
8-Lead Hermetic DIP (Z)	148	16	°C/W
8-Lead Plastic DIP (P)	103	43	°C/W
8-Lead SO (S)	158	43	°C/W

NOTES

¹For supply voltages less than 22 V, the absolute maximum input voltage is equal to the supply voltage.

²The OP37's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds 0.7 V, the input Current should be limited to 25 mA.

³ θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

⁴Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ORDERING GUIDE

$T_A = 25^\circ\text{C}$ $V_{OS\ MAX}$ (μV)	CerDIP 8-Lead	Plastic 8-Lead	Operating Temperature Range
25	OP37AZ*		MIL
25	OP37EZ	OP37EP	IND/COM
60		OP37FP*	IND/COM
100		OP37GP	XIND
100	OP37GZ	OP37GS	XIND

*Not for new design, obsolete, April 2002.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP37 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



SPECIFICATIONS ($V_S = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	OP37A/E			OP37F			OP37G			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{OS}	Note 1	10	25		20	60		30	100	μV	
Long-Term Stability	V_{OS}/Time	Notes 2, 3	0.2	1.0		0.3	1.5		0.4	2.0	$\mu\text{V}/\text{Mo}$	
Input Offset Current	I_{OS}		7	35		9	50		12	75	nA	
Input Bias Current	I_B		± 10	± 40		± 12	± 55		± 15	± 80	nA	
Input Noise Voltage	e_{np-p}	1 Hz to 10 Hz ^{3, 5}	0.08	0.18		0.08	0.18		0.09	0.25	$\mu\text{V p-p}$	
Input Noise Voltage Density	e_n	$f_0 = 10\text{ Hz}^3$ $f_0 = 30\text{ Hz}^3$ $f_0 = 1000\text{ Hz}^3$	3.5 3.1 3.0	5.5 4.5 3.8		3.5 3.1 3.0	5.5 4.5 3.8		3.8 3.3 3.2	8.0 5.6 4.5	$\text{nV}/\sqrt{\text{Hz}}$	
Input Noise Current Density	i_N	$f_0 = 10\text{ Hz}^3, 6$ $f_0 = 30\text{ Hz}^3, 6$ $f_0 = 1000\text{ Hz}^3, 6$	1.7 1.0 0.4	4.0 2.3 0.6		1.7 1.0 0.4	4.0 2.3 0.6		1.7 1.0 0.4	0.6	$\text{pA}/\sqrt{\text{Hz}}$	
Input Resistance Differential Mode	R_{IN}	Note 7	1.3	6		0.9	4.5		0.7	4	M Ω	
Input Resistance Common Mode	R_{INCM}		3			2.5			2		G Ω	
Input Voltage Range	IVR		± 11	± 12.3		± 11	± 12.3		± 11	± 12.3	V	
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11\text{ V}$	114	126		106	123		100	120	dB	
Power Supply Rejection Ratio	PSSR	$V_S = \pm 4\text{ V}$ to $\pm 18\text{ V}$	1	10		1	10		2	20	$\mu\text{V}/\text{V}$	
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2\text{ k}\Omega$, $V_O = \pm 10\text{ V}$ $R_L \geq 1\text{ k}\Omega$, $V_O = \pm 10\text{ V}$ $R_L \geq 600\ \Omega$, $V_O = \pm 1\text{ V}$, $V_S \pm 4^4$	1000 800 250	1800 1500 700		1000 800 250	1800 1500 700		700 400 200	1500 1500 500	V/mV V/mV V/mV	
Output Voltage Swing	V_O	$R_L \geq 2\text{ k}\Omega$ $R_L \geq 600\ \Omega$ $R_L \geq 2\text{ k}\ \Omega^4$	± 12.0 ± 10 11	± 13.8 ± 11.5 17		± 12.0 ± 10 11	± 13.8 ± 11.5 17		± 11.5 ± 10 11	± 13.5 ± 11.5 17	V V V/ μs	
Slew Rate	SR		11	17		11	17		11	17	V/ μs	
Gain Bandwidth Product	GBW	$f_0 = 10\text{ kHz}^4$ $f_0 = 1\text{ MHz}$	45 40	63 40		45 40	63 40		45 40	63 40	MHz MHz	
Open-Loop Output Resistance	R_O	$V_O = 0, I_O = 0$	70			70			70		Ω	
Power Consumption	P_d	$V_O = 0$	90	140		90	140		100	170	mW	
Offset Adjustment Range		$R_p = 10\text{ k}\Omega$	± 4			± 4			± 4		mV	

NOTES

- ¹Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.
- ²Long term input offset voltage stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5 μV —refer to typical performance curve.
- ³Sample tested.
- ⁴Guaranteed by design.
- ⁵See test circuit and frequency response curve for 0.1 Hz to 10 Hz tester.
- ⁶See test circuit for current noise measurement.
- ⁷Guaranteed by input bias current.

OP37—SPECIFICATIONS

Electrical Characteristics ($V_S = \pm 15\text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	OP37A			OP37C			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{OS}	Note 1		10	25		30	100	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSN}	Note 2 Note 3		0.2	0.6		0.4	1.8	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{OS}			15	50		30	135	nA
Input Bias Current	I_B			± 20	± 60		± 35	± 150	nA
Input Voltage Range	IVR		± 10.3	± 11.5		± 10.2	± 11.5		V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10\text{ V}$	108	122		94	116		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5\text{ V}$ to $\pm 18\text{ V}$		2	16		4	51	$\mu\text{V}/\text{V}$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2\text{ k}\Omega$, $V_O = \pm 10\text{ V}$	600	1200		300	800		V/mV
Output Voltage Swing	V_O	$R_L \geq 2\text{ k}\Omega$	± 11.5	± 13.5		± 10.5	± 13.0		V

Electrical Characteristics ($V_S = \pm 15\text{ V}$, $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for OP37EZ/FZ, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ for OP37EP/FP, and $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for OP37GP/GS/GZ, unless otherwise noted.)

Parameter	Symbol	Conditions	OP37E			OP37F			OP37C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{OS}			20	50		40	140		55	220	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSN}	Note 2 Note 3		0.2	0.6		0.3	1.3		0.4	1.8	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{OS}			10	50		14	85		20	135	nA
Input Bias Current	I_B			± 14	± 60		± 18	± 95		± 25	± 150	nA
Input Voltage Range	IVR		± 10.5	± 11.8		± 10.5	± 11.8		± 10.5	± 11.8		V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10\text{ V}$	108	122		100	119		94	116		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5\text{ V}$ to $\pm 18\text{ V}$		2	15		2	16		4	32	$\mu\text{V}/\text{V}$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2\text{ k}\Omega$, $V_O = \pm 10\text{ V}$	750	1500		700	1300		450	1000		V/mV
Output Voltage Swing	V_O	$R_L \geq 2\text{ k}\Omega$	± 11.7	± 13.6		± 11.4	± 13.5		± 11	± 13.3		V

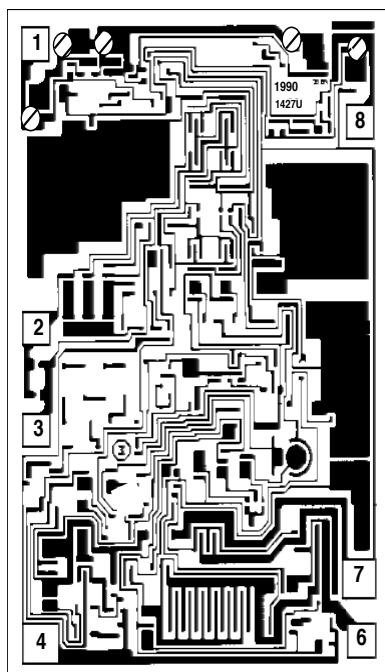
NOTES

¹Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.

²The $TC_{V_{OS}}$ performance is within the specifications unnullled or when nullled with $R_p = 8\text{ k}\Omega$ to $20\text{ k}\Omega$. $TC_{V_{OS}}$ is 100% tested for A/E grades, sample tested for F/G grades.

³Guaranteed by design.

BINDING DIAGRAM



- 1. NULL
- 2. (-) INPUT
- 3. (+) INPUT
- 4. V-
- 6. OUTPUT
- 7. V+
- 8. NULL

Wafer Test Limits ($V_S = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$ for OP37N, OP37G, and OP37GR devices; $T_A = 125^\circ\text{C}$ for OP37NT and OP37GT devices, unless otherwise noted.)

Parameter	Symbol	Conditions	OP37NT Limit	OP37N Limit	OP37GT Limit	OP37G Limit	OP37GR Limit	Unit
Input Offset Voltage	V_{OS}	Note 1	60	35	200	60	100	$\mu\text{V MAX}$
Input Offset Current	I_{OS}		50	35	85	50	75	nA MAX
Input Bias Current	I_B		± 60	± 40	± 95	± 55	± 80	nA MAX
Input Voltage Range	IVR		± 10.3	± 11	± 10.3	± 11	± 11	V MIN
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11\text{ V}$	108	114	100	106	100	dB MIN
Power Supply Rejection Ratio	PSRR	$T_A = 25^\circ\text{C}$, $V_S = \pm 4\text{ V to } \pm 18\text{ V}$	10	10	10	10	20	$\mu\text{V/V MAX}$
		$T_A = 125^\circ\text{C}$, $V_S = \pm 4.5\text{ V to } \pm 18\text{ V}$	16		20			$\mu\text{V/V MAX}$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2\text{ k}\Omega$, $V_O = \pm 10\text{ V}$	600	1000	500	1000	700	V/mV MIN
		$R_L \geq 1\text{ k}\Omega$, $V_O = \pm 10\text{ V}$		800		800		V/mV MIN
Output Voltage Swing	V_O	$R_L \geq 2\text{ k}\Omega$ $R_L \geq 600\text{ k}\Omega$	± 11.5	± 12 ± 10	± 11	± 12 ± 10	± 11.5 ± 10	V MIN V MIN
Power Consumption	P_d	$V_O = 0$		140		140	170	mW MAX

NOTES

For 25°C characteristics of OP37NT and OP37GT devices, see OP37N and OP37G characteristics, respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

OP37

Typical Electrical Characteristics ($V_S = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

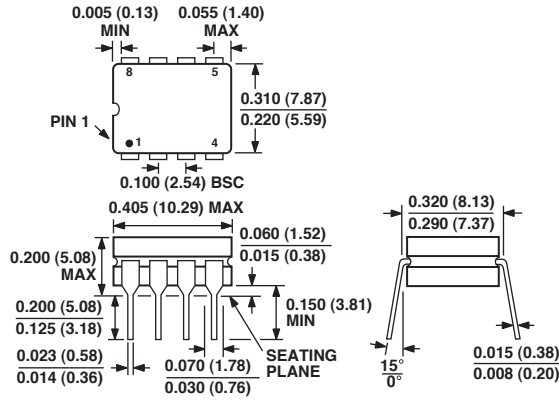
Parameter	Symbol	Conditions	OP37NT Typical	OP37N Typical	OP37GT Typical	OP37G Typical	OP37GR Typical	Unit
Average Input Offset Voltage Drift	TCV_{OS} or TCV_{OSN}	Nulled or Unnulled $R_P = 8\text{ k}\Omega$ to $20\text{ k}\Omega$	0.2	0.2	0.3	0.3	0.4	$\mu\text{V}/^\circ\text{C}$
Average Input Offset Current Drift	TCI_{OS}		80	80	130	130	180	$\text{pA}/^\circ\text{C}$
Average Input Bias Current Drift	TCI_B		100	100	160	160	200	$\text{pA}/^\circ\text{C}$
Input Noise Voltage Density	e_n	$f_0 = 10\text{ Hz}$	3.5	3.5	3.5	3.5	3.8	$\text{nV}/\sqrt{\text{Hz}}$
		$f_0 = 30\text{ Hz}$	3.1	3.1	3.1	3.1	3.3	$\text{nV}/\sqrt{\text{Hz}}$
		$f_0 = 1000\text{ Hz}$	3.0	3.0	3.0	3.0	3.2	$\text{nV}/\sqrt{\text{Hz}}$
Input Noise Current Density	i_n	$f_0 = 10\text{ Hz}$	1.7	1.7	1.7	1.7	1.7	$\text{pA}/\sqrt{\text{Hz}}$
		$f_0 = 30\text{ Hz}$	1.0	1.0	1.0	1.0	1.0	$\text{pA}/\sqrt{\text{Hz}}$
		$f_0 = 1000\text{ Hz}$	0.4	0.4	0.4	0.4	0.4	$\text{pA}/\sqrt{\text{Hz}}$
Input Noise Voltage	$e_{n\text{ p-p}}$	0.1 Hz to 10 Hz	0.08	0.08	0.08	0.08	0.09	$\mu\text{V p-p}$
Slew Rate	SR	$R_L \geq 2\text{ k}\Omega$	17	17	17	17	17	$\text{V}/\mu\text{s}$
Gain Bandwidth Product	GBW	$f_0 = 10\text{ kHz}$	63	63	63	63	63	MHz

OUTLINE DIMENSIONS

8-Lead Ceramic DIP – Glass Hermetic Seal [CERDIP]

(Q-8)

Dimensions shown in inches and (millimeters)

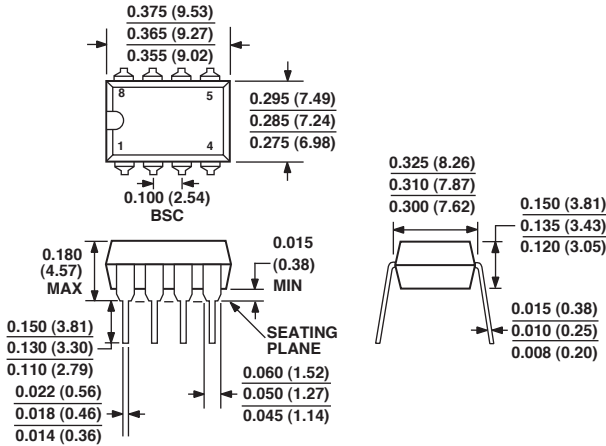


CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Plastic Dual-in-Line Package [PDIP]

(N-8)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095AA

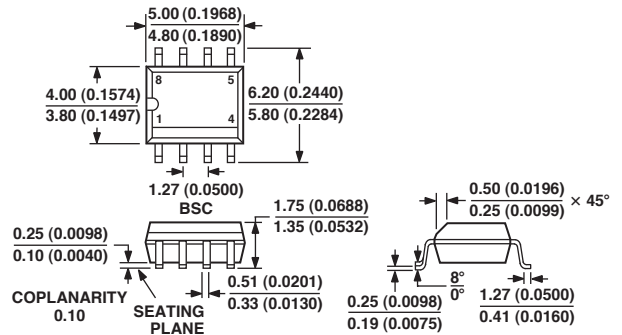
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Standard Small Outline Package [SOIC]

Narrow Body

(RN-8)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA

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